REMARKS

Entry of the foregoing, reexamination and reconsideration of the subject matter identified in caption, as amended, pursuant to and consistent with 37 C.F.R. §1.112, and in light of the remarks which follow are respectfully requested.

Claims 1-35 are pending in the application, claims 33-35 having been newly added above. Claims 33 and 34 find support at least in sections [0025], [0135] and Figure 2 of the application, and claim 35 finds support at least in original claim 20 and section [0150].

By the foregoing amendments, claim 32 has been revised in response to the §112, second paragraph rejection by further pointing out that the lid hermetically seals the optical device. Support can be found at least in section [0190] of the application.

Turning now to the Official Action, claim 32 stands rejected under 35 U.S.C. §112, second paragraph. This rejection has been obviated by the foregoing amendment to claim 32. Accordingly, withdrawal of this rejection is respectfully requested.

Claims 1, 7, 8, 10, 12, 13, 20 and 22 stand rejected under 35 U.S.C. §102(b) as being anticipated by Jacobowitz et al (U.S. Patent No. 5,333,225). In addition, claims 2-6, 9, 11, 14-19, 21 and 23-32 stand rejected under 35 U.S.C. §103(a) as being obvious over Jacobowitz et al in view of Sakaino et al (U.S. Patent No. 5,909,523). These rejections are completely improper and should be withdrawn.

The present invention relates to optical submounts and to optical devices. Independent claim 1, for example, sets forth an optical submount comprising: a) a substrate; b) a trench in the substrate for holding an optoelectronic device on-edge; c) an electrical connection pit adjoining the trench; and d) a metallization layer in the electrical connection pit.

Independent claim 20 sets forth an optical device, comprising: a) a substrate; b) a trench in the substrate; c) an electrical connection pit adjoining the trench; d) a metallization layer in the electrical connection pit; and e) an optoelectronic device disposed on-edge in the trench, wherein the optoelectronic device has a contact pad soldered to the metallization layer.

The present claims cannot properly be rejected based on the teachings of Jacobowitz et al alone or in view of Sakaino et al.

Jacobowitz et al relates to apparatus and methods for embedding one or more optical fiber connectors into a multilayer single-chip module or multi-chip module, or into a thermal conduction module with integrated photonic receivers and transmitters (col. 1, lines 40-44).

It is well established, that in order to establish anticipation under §102(b), each element of the claim in issue must be found, either expressly described or under principles of inherency, in a single prior art reference. Kalman v. Kimberly-Clark Corp., 218 USPQ 789 (Fed. Cir. 1983). That is not the case here.

Jacobowitz et al does not disclose or suggest each and every feature of applicants' invention. For example, Jacobowitz et al does not disclose or fairly suggest a trench in the substrate for holding an optoelectronic device on-edge, as set forth in claim 1, or an optoelectronic device disposed on-edge in a trench in a substrate, as set forth in independent claim 20. In this regard, the Examiner relies on Figure 4 of Jacobowitz et al for that document's purported disclosure of "a trench 33 in the substrate 4 for holding an optoelectronic device 19 on-edge" (Official Action, page 2). Well 33 of Jacobowitz et al's Figure 4 is not for holding an optoelectronic device. What the Examiner refers to as "optoelectronic device 19" is not an optoelectronic device at all. More specifically, Jacobowitz et al describes silicon optical subassembly receptacle member 19 at column 8, line 8 to column 9, line 6 with reference to Figure 3, which shows an exploded view of member 19. The structure includes, *inter alia*, an upper silicon chip 24, a lower silicon chip 22 and optical fibers 21 mounted and bonded into the lower silicon chip 22. Optical subassembly receptacle member 19 includes optical but no electrical functionality. Accordingly, this structure cannot properly be deemed an optoelectronic device.

Nor is the Jacobowitz et al optical subassembly receptacle member 19 held on-edge in the well 33 of Figure 4. As discussed in the subject application, optoelectronic devices, for example, surface emitting or surface detecting devices such as vertical cavity surface emitting lasers or photodetectors, require a geometry other than being disposed flat on a submount chip. Applicants have addressed this need by providing structures in which such optoelectronic devices can be held on edge. The Jacobowitz et al optical subassembly receptacle member 19 is held flat, rather than on edge.

Jacobowitz et al further does not disclose or fairly suggest an electrical connection pit adjoining the trench or a metallization layer in an electrical connection pit, as recited in claims 1 and 20. The Examiner, again relying on Figure 4 of Jacobowitz et al, takes the position that the document discloses "electrical connection pit 34 adjoining the trench" and "a metallization layer in the electrical connection pit (col. 9, ll. 22-25)" (Official Action, page 4). Applicants respectfully disagree with the Examiner's position.

With reference to Figure 4, Jacobowitz et al discloses an array of metal pads 34 at the bottom of well 33 for reflow bonding to a corresponding pad array on the underside of silicon receptacle structure 19 These metal pads 34 are to allow bonding of the optical subassembly receptacle member 19 to the substrate 4, and are not for electrical connectivity. As explained above, structure 19 of Jacobowitz et al has optical but no electrical functionality.

For at least the foregoing reasons, the §102 rejection based on Jacobowitz et al is improper and should be withdrawn.

Furthermore, Sakaino et al fails to cure the above-described deficiencies in Jacobowitz et al. Sakaino et al relates to an optical module in which an optical fiber or an optical waveguide is optically coupled with an optical semiconductor device, employed in an optical transmitter or receiver (col. 1, lines 5-8). The Examiner relies on Sakaino et al for that document's purported disclosure of a groove in a substrate, a lid and enclosing the structure in a protective package (Official Action at page 4). However, even if one would have combined the documents in the manner suggested in the Official Action, the present invention would not result. Simply put, no *prima facie* case of obviousness has been established.

Accordingly, withdrawal of the §102 rejection based on Jacobowitz et al and the §103(a) rejection based on Jacobowitz et al in view of Sakaino et al is respectfully requested.

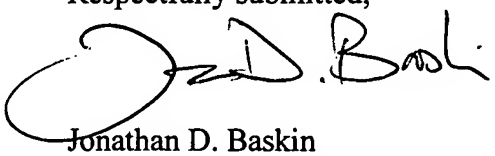
As a final matter, newly presented claims 33 and 34 depend from claim 20, and are allowable over the applied documents at least for the reasons set forth above with respect to claim 20, and further distinguish over the documents. Those claims recite that the optoelectronic device is a surface emitting or detecting device (claim 33), and that the optoelectronic device has an optical plane in a direction parallel to the surface of

the substrate in which the trench is formed (claim 34). Claim 35 is allowable at least for the reasons set forth above with respect to claim 20.

From the foregoing, further and favorable action in the form of a Notice of Allowance is believed to be next in order, and such action is earnestly solicited.

If there are any questions concerning this paper or the application in general, the Examiner is invited to telephone the undersigned at her earliest convenience.

Respectfully submitted,



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